REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 15, 19 and 38-72 are in this application. Claims 15, 51-53, 56-57, 60, 62, and 65 have been amended. Claims 15 and 51-53, 57, and 62 have been amended to clarify the claims. Claims 56, 60, and 65 have been amended to alternately claim the present invention. Claims 67-72 have been added to additionally claim the present invention. Claims 40-44 have been allowed. Applicant requests the Examiner to indicate whether the formal drawings submitted on September 9, 2002 have been entered into the case. Applicant further requests the Examiner to indicate if the power of attorney submitted on July 22, 2002 has been entered into the case.

The Examiner rejected claims 15, 19, 38-39, 45-57, 60-62, and 65-66 under 35 U.S.C. §103(a) as being unpatentable over Gens et al. (U.S. Patent No. 5,515,225) considered alone, or in view of the Admitted Prior Art (APA). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 15 recites, in part,

> "a plurality of pads; [and]
> "a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad. [Brackets added.]

Claim 57 recites similar limitations.

In rejecting the claims, the Examiner pointed to pads P1 and P2 shown in FIG. 3 of Gens as constituting the plurality of pads. In addition, the Examiner pointed to the horizontal lines, which are connected to the right side of the high power supply terminals labeled VDD1 and VDD2 (and the vertical extensions connected to the horizontal lines and the diodes) as constituting the plurality of positive lines in Gen's structure.

Applicant notes, however, that the Gens reference expressly teaches that the boxes P1, P2, VDD1, VDD2, VSS1, and VSS2 are pads. (Boxes P1 and P2 are I/O pads, boxes VDD1 and VDD2 are power supply pads, and boxes VSS1 and VSS2 are ground pads.) In addition,

FIG. 3 of Gens shows that the horizontal lines are directly connected to boxes VDD1 and VDD2. Since the horizontal lines shown in FIG. 3 of Gens are directly connected to pads VDD1 and VDD2, it is not possible for the horizontal lines to be read to be the positive lines required by claims 15 and 57.

In response, the Examiner acknowledged that Gens teaches that box VDD1 is a voltage pad. However, the Examiner argued that if the first and second diodes are considered to be connected to positive and negative voltages, where the I/O pad is connected in between the diodes and not directly connected to a pad, then the positive lines of Gens are not directly connected to a pad.

Applicant respectfully does not understand the Examiner's argument. Claims 15 and 57 require that none of the positive lines be directly connected to a pad. The phrase "a pad" is not limited to any particular type of pad. As a result, a structure which is directly connected to a pad can not be read to be a positive line. Since the horizontal lines (read to be the plurality of positive lines) shown in FIG. 3 of Gens are directly connected to pads VDD1 and VDD2, the horizontal lines can not be read to be the plurality of positive lines required by claims 15 and 57.

The Examiner also argued, noting that the specification can be used in interpreting claim language when the specification provides definitions for claim terms, that the term "pad" is defined in the specification as an I/O pad. As a result, the Examiner argued that a voltage pad can not be read to be an I/O pad.

Applicant notes, however, that while

> "the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification." (See MPEP §2111.01 citing In re Zletz, 893 F.2d 319 (Fed. Cir. 1989).)

From what applicant can determine, the Examiner is not questioning the plain meaning of the term "pad" to one skilled in the art, but instead is arguing that applicant's specification defines the term "pad" to be only an I/O pad.

Applicant further notes that one

> "must bear in mind that . . . the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification. It is only when the specification provides definitions for terms appearing in the claims that the specification can be used in interpreting claim language." (See MPEP §2111.01)

However, the Examiner has not identified, and applicant can not find, where applicant's specification defines the term "pad" to be only an I/O pad.

Further, applicant notes that applicant's specification teaches:

> "[I]n operation, I/O pins 110 and 112 either receive signals that have been output by an external driver, such as driver 114, or output signals that have been received from an internal driver, such as internal driver 116." (See page 2, lines 7-11 of applicant's specification.)

> "The main disadvantages of the prior ESD art is that ESD protection of multiple isolated VCC lines and multiple isolated ground lines is not possible." (See page 15, lines 7-11 of applicant's specification.)

Thus, applicant's specification teaches that I/O pads (pins) either receive signals that have been output by an external driver, or output signals that have been received from an internal driver. In addition, applicant's specification also teaches that prior ESD art can not protect VCC pads (lines) and ground pads (lines).

However, applicant's specification further teaches that:

> "by utilizing the current invention, chip 1200 provides ESD protection for all I/O pins, including multiple isolated power supplies and multiple isolated grounds." (See page 23, lines 2-6 of applicant's specification.)

Thus, applicant's specification expressly teaches that the present invention provides ESD protection for I/O pads, VCC pads, and ground pads.

Applicant's specification additionally teaches:

> "FIG. 16 shows a circuit diagram which illustrates a chip 1600 that employs an alternate form of the present invention. As shown in FIG. 16, chip 1600 includes . . . a plurality of pads 1620." (See from page 33, line 24 to page 34, line 1 of applicant's specification.)

Thus, FIG. 16 shows an alternate form of the present invention which, as just noted, provides ESD protection for I/O pads, VCC pads, and ground pads. In addition, applicant has been unable to find anything that teaches that the FIG. 16 embodiment differs from the FIG. 12 embodiment because the FIG. 16 embodiment applies only to I/O pads and not VCC and ground pads.

Further, the specification expressly states that chip 1600 includes a plurality of pads 1620. Since the phrase "a plurality of pads" is not restrictive, and there is no indication that the FIG. 16 embodiment excludes one of the significant advantages of the FIG. 12 embodiment, namely providing protection for I/O pads, VCC pads, and ground pads, the phrase "a plurality of pads" can be read to include more than just I/O pads.

Applicant further notes that the specification states:

> "[i]f any one of the I/O pads 1620 in FIG. 16 is zapped positively with respect to a second I/O pad 1620, an ESD current will flow between the two I/O pads being zapped." (See page 34, lines 22-26 of applicant's specification.)

The above portion of the specification does not teach that pads 1620 are only I/O pads, but is merely an example of what happens when one I/O pad is zapped positively with respect to a second I/O pad.

Thus, since applicant's specification does not define the term "pad" to mean only an I/O pad, the Examiner must use the plain meaning of the term "pad" (as understood by one skilled in the art). Using the plain meaning of the term "pad," the horizontal lines shown in

FIG. 3 of Gens can not be read to be the positive lines of the claims because these lines are connected to pads, the VCC1 and VCC2 pads.

As a result, claims 15 and 57 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA). In addition, since claims 19, 58-61, and 69-70 directly or indirectly depend from claims 15 and 57, claims 19, 58-61, and 69-70 are patentable over Gens for the same reasons as claims 15 and 57.

With respect to claim 45, this claim recites that the ESD positive lines are never connected to a steady voltage source. However, as shown in FIGs. 2 and 3 of Gens, the positive (horizontal) lines are connected to the VDD1 and VDD2 pads. As a result, whenever power is applied to the device, the positive (horizontal) lines are connected to a steady voltage source. Thus, claim 45 is patentable over Gens, and Gens in view of the APA for this additional reason as well.

With respect to claims 58 and 63, these claims are patentable over Gens, and Gens in view of the APA for the same reason that the Examiner allowed claim 40, i.e., the structure of the first diode.

With respect to new claims 69-72, these claims recite that a second diode is directly connected to a pad and directly connected to a positive line (contrasted with the term "connected" that the Examiner has read not to require a direct connection). FIGs. 2 and 3 of Gens, however, do not show a second diode (D1) that is directly connected to a pad (P1 or P2) and a positive (horizontal) line. Rather, FIGs. 2 and 3 of Gens shows that two diodes lie between a pad (P1 or P2) and a positive line. Thus, claims 69-72 are patentable over Gens, and Gens in view of the APA for this further reason.

With respect to independent claim 51, this claim recites, in part,

> "a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring . . . a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate."

Claim 62 recites similar limitations.

In rejecting the claims, the Examiner pointed to the lower diodes (D2) connected between the ESD positive lines (the horizontal lines connected to the VDD1 and VDD2 pads) and the ESD negative ring as constituting the plurality of switches required by claims 51 and 62. However, with reference to FIGs. 2 and 3 of Gens, a current will not flow from a positive line (e.g., a horizontal line connected to the VDD1 pad) through a lower diode (D2) to the negative ring (R2) when a voltage on the positive line rises at a first rate. Instead, a current will flow from the positive line (e.g., a horizontal line connected to the VDD1 pad) through the upper diode (D1) and then to the negative ring (R2) via the zener diode (Z). As a result, the lower diodes (D2) shown in FIGs. 2 and 3 of Gens can not be read to be the switches required by claims 51 and 62.

The Examiner also stated that Gens does not explicitly state that the plurality of switches are connected between the ESD positive lines and the ESD negative ring, but argued that this feature is inherent in Gens because it is well known in the art that diodes are switches. However, "[i]nherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." [Brackets added.] In re Oelrich, 666 F.2d 578, 581 (CCPA 1981).

Thus, inherency exists only where the result will always occur. In the present case, the Examiner has provided no evidence to show that the lower diodes (D2) in Gens ever function as a switch that passes a current from a positive line to the negative ring. As a result, the Examiner has not established that the lower diodes (D2) shown in Gens may inherently be read to be switches.

Alternately, the Examiner pointed to the transistor shown in FIGs. 1 and 2 of the APA that is connected to the VCC wire 120 and the ground wire 122 as constituting a switch that passes a current from the positive line (VCC wire 120) to the negative ring (ground wire 122) when a voltage on the positive line rises at a first rate. The Examiner then appears to argue that it would be obvious to connect the transistor of the APA in lieu of the lower diodes (D2) to provide a more effective unidirectional flow of current during an ESD operation.

As noted above, when an ESD event occurs in Gens, a current flows from the positive line (e.g., a horizontal line connected to the VDD1 pad) through the upper diode (D1) and

then to the negative ring (R2) via the zener diode (Z). Making the substitution suggested by the Examiner would prevent the Gens circuit from operating as intended because the current would no longer flow from the positive line through the upper diode (D1) and then to the negative ring (R2) via the zener diode (Z), but instead would apparently flow directly from the positive line (e.g., a horizontal line connected to the VDD1 pad) through the transistor directly to the negative ring (R2). Since one skilled in the art would not be motivated to alter a structure to prevent it from being used in its intended way, one skilled in the art would not be motivated to make the combination suggested by the Examiner.

As a result, claims 51 and 62 are patentable over Gens, and Gens in view of the Admitted Prior Art (APA). In addition, since claims 52-56, 63-66, and 71-72 directly or indirectly depend from claims 51 and 62, respectively, claims 52-56, 63-66, and 71-72 are patentable over Gens for the same reasons as claims 51 and 62.

The Examiner objected to claims 58, 59, 63, and 64 as being dependent upon a rejected base claim, but indicated that claims 58, 59, 63, and 64 would be allowable if rewritten to be in independent form and to include all of the limitations of any intervening claims. New claim 67 has been added and is believed to include the limitations of claims 57 and 58, and new claim 68 has been added and is believed to include the limitations of claims 62 and 63.

The Examiner also indicated that claims 15 and 51 would be allowable if the phrase "each second diode being connected between a pad and a positive line" would read "only one second diode being connected between each pad and each positive line." The Examiner further indicated that claims 57 and 62 would be allowable if the phrase "only one second diode being connected between a pad and a positive line" would read "only one second diode being connected between each pad and each positive line."

Applicant respectfully notes, however, that applicant's disclosure does not appear to support the suggested claim language. As shown in FIG. 16, applicant does not teach that a single second diode 1635 is connected between each pad 1620. Rather, FIG. 16 shows that two second diodes (connected to the same positive line) are connected between each pad. Further, FIG. 16 does not show that a single second diode 1635 is connected between each

positive line 1640-1647. Rather, FIG. 16 shows that two second diodes (and two first diodes 1630) are connected between each positive line 1640-1647. Thus, since the suggested claim language does not appear to be supported by the specification, applicant has not amended claims 15, 51, 57, and 62 to include these limitations.

During a telephonic interview, applicant's attorney understood that claims 15 and 51 would be allowable if amended to recite that only one second diode is connected between a pad and a positive line. New claims 57 and 62 were added, and believed to recite the limitations suggested by the Examiner which would make claims 15 and 51, respectively, allowable.

The Examiner has since indicated that there must have been some misunderstanding. As a result, applicant has amended claims 57 and 62 to alternately and additionally claim the present invention, and requests that amended claims 57-66 be considered as first presented, and not as being amended to overcome art of record. Further, claim 62 was also amended to recite a second rate to add further clarity to the claim.

Applicant has also discovered a counting error with respect to the number of times that claim 15 has been amended. The error has been corrected in the present amendment. Claim 15 has been amended six previous times (8/15/00; 12/2700; 9/4/01; 1/16/02; 5/7/02; and 9/25/02), and is amended for the seventh time in the present amendment.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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APPENDIX

In the Claims

Please amend the claims as follows:

15. (Seventh Amendment) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each [positive line is connected to the negative ring via an] ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

51. (Twice Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each [positive line is connected to the negative ring via an] ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD

switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

52. (Twice Amended) The chip of claim 51 wherein the [switches block] switch blocks a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

53. (Twice Amended) The chip of claim 51 wherein [the second diodes are] a second diode is forward biased when the voltage on the positive line rises at the second rate.

56. (Amended) The chip of claim 51 wherein [the ESD switches are not connected to a pad] an ESD switch is directly connected to a positive line and the negative ring.

57. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each [positive line is connected to the negative ring via an] ESD switch is connected to a positive line and the ESD negative ring;

a plurality of first diodes connected [to the pads] so that each first diode is connected [to] between a pad and the negative ring; and

a plurality of second diodes connected [to the pads] so that [only one] each second diode is connected between a pad and a positive line.

60. (Amended) The semiconductor chip of claim 57 wherein [the ESD switches are not directly connected to a pad] an ESD switch is directly connected to a positive line and the negative ring.

62. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each [positive line is connected to the negative ring via an] ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate that is faster than a second rate;

a plurality of first diodes connected [to the pads] so that each first diode is connected [to] between a pad and the negative ring; and

a plurality of second diodes connected [to the pads] so that [only one] each second diode is connected between a pad and a positive line.

65. (Amended) The semiconductor chip of claim 62 wherein [the ESD switches are not directly connected to a pad] an ESD switch is directly connected to a positive line and the negative ring.

Claims 67-72 have been added.